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EXAMINER
VU, HUNG K

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,686	PEPE ET AL.	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-16 and 33-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13,14 and 33-42* is/are rejected.

7)☒ Claim(s) *15,16,43 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 1, 9, 14, 33, 37 and 42 are objected to because of the following informalities:

In claim 1, line 7, "prepared" should be changed to "pre-formed" for clarity.

In claim 9, line 5, "prepared" should be changed to "pre-formed" for clarity.

In claim 11, line 4, "said integral" should be changed to "an integral" for clarity.

In claim 14, line 1, delete "and" for clarity.

In claim 33, line 8, a period "." should be changed to a semicolon ";" for clarity.

In claim 33, line 10, "prepared" should be changed to "pre-formed" for clarity.

In claim 37, line 5, "prepared" should be changed to "pre-formed" for clarity.

In claim 39, line 4, "said integral" should be changed to "an integral" for clarity.

In claim 42, line 1, delete "and" for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 33-39 and 41-42 are rejected under 35 U.S.C. 102(a) as being anticipated by Kwon et al. (PN 6,235,552, of record).

Kwon et al. discloses, as shown in Figures 19-20 and 26-27, a method of preparing a pre-formed integrated circuit chip for encapsulation in an electronic package comprising the steps of:

forming an interconnect assembly (130) separately from the pre-formed integrated circuit chip (100); (note Figures 6 and 14-15), and forming the interconnect assembly including the steps of:

forming at least one pad (116) in a plurality of stacked interconnect layers, each of which at least one pad in each interconnect layer can be accessed and electrically connected on opposing side of the pad. Note that the pad is capable to function as a test pad;

forming a plurality of conducive bumps (128) connected to the terminals (104) of the pre-formed integrated circuit chip,

bonding the interconnect assembly to the pre-formed integrated circuit chip; (note Figure 16)

passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into an integral structure to provide the electronic package. (note Figures 17 and 26-27)

With regard to claim 34, Kwon et al. discloses the at least one test pad forms a test pad having gold on a conductive field metal. (note Col. 3, lines 14-33 and lines 44-48)

With regard to claim 35, Kwon et al. discloses the step of forming the plurality of conductive bumps connected to the terminals of the integrated circuit chip forms a metallic bump making connecting to a terminal o the integrated circuit chip and a solder layer (108) disposed on the metallic bump.

With regard to claim 36, Kwon et al. discloses the step of forming the interconnect assembly comprises forming at least one pad (116) in an interconnect layer, which at least one pad can be accessed and electrically connected on opposing side of the pad, and wherein the step of bonding the interconnect assembly to the pre-formed integrated circuit chip flip bonds the solder layer onto one side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 37, Kwon et al. discloses the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises underfilling the pre-formed integrated circuit chip with an insulating material (134,156) to remove all voids between the pre-formed integrated circuit chip and the interconnect assembly.

With regard to claims 38 and 39, Kwon et al. discloses the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises potting (by layer 156) the interconnect assembly and the pre-formed integrated circuit chip into an integral package.

With regard to claim 41, Kwon et al. discloses the method further comprising a step of accessing the pre-formed integrated circuit chip through electrical connect to at least one pad through a surface thereof opposing the surface of the at least one pad contacting a terminal of the pre-formed integrated circuit chip. Note that the pad is capable to function as a test pad. Also, the pad is capable to use to test the pre-formed integrated circuit chip. (note Figures 18-20, 27 and 31)

With regard to claim 42, Kwon et al. discloses the method further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein the plurality of interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing the plurality of electronic packages from each other. (note Figures 20 and 26)

3. Claims 1, 3, 5, 9, 10, 11, 13 and 37-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Murayama et al. (PN 6,548,330).

Murayama et al. discloses, as shown in Figures 5 and 12, a method of preparing a pre-formed integrated circuit chip for encapsulation in an electronic package comprising the steps of:

forming an interconnect assembly (2) separately from the pre-formed integrated circuit chip (10); (note Figures 2-3 and 8-9)

forming a plurality of conducive bumps (no label) connected to the terminals (10) of the pre-formed integrated circuit chip,

bonding the interconnect assembly to the pre-formed integrated circuit chip; (note Figures 3 and 9)

passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into an integral structure to provide the electronic package; (note Figures 4 and 11)

thinning the pre-formed integrated circuit chip to provide the electronic package. (note Figure 5 and 12 and Col. 5, lines 9-13)

With regard to claim 3, Murayama et al. discloses the step of forming the interconnect assembly comprises forming at least one pad (5,6) in an interconnect layer, which at least one pad can be accessed and electrically connected on opposing side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 5, Murayama et al. discloses the step of forming the interconnect assembly comprises forming at least one pad (5,6) in a plurality of stacked interconnect layers (5,6,7) each of which at least one pad in each interconnect layer can be accessed and electrically connected on opposing side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 9, Murayama et al. discloses the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises underfilling the pre-formed integrated circuit chip with an insulating material (11) to remove all voids between the pre-formed integrated circuit chip and the interconnect assembly.

With regard to claims 10 and 11, Murayama et al. discloses the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises potting (by layer 11) the interconnect assembly and the pre-formed integrated circuit chip into an integral package.

With regard to claim 13, Murayama et al. discloses the method further comprising a step of accessing the pre-formed integrated circuit chip through electrical connect to at least one pad through a surface thereof opposing the surface of the at least one pad contacting a terminal of the pre-formed integrated circuit chip. Note that the pad is capable to function as a test pad. Also, the pad is capable to use to test the pre-formed integrated circuit chip. (note Figures 6 and 12)

With regard to claim 37, Murayama et al. discloses the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises underfilling the pre-formed integrated circuit chip with an insulating material (134,156) to remove all voids between the pre-formed integrated circuit chip and the interconnect assembly.

With regard to claims 38 and 39, Murayama et al. discloses the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises potting (by layer 156) the interconnect assembly and the pre-formed integrated circuit chip into an integral package.

With regard to claim 40, Murayama et al. discloses the method further comprising the step thinning the pre-formed integrated circuit chip. (See Figures 5 and 12)

With regard to claim 41, Murayama et al. discloses the method further comprising a step of accessing the pre-formed integrated circuit chip through electrical connect to at least one pad through a surface thereof opposing the surface of the at least one pad contacting a terminal of the pre-formed integrated circuit chip. Note that the pad is capable to function as a test pad. Also, the pad is capable to use to test the pre-formed integrated circuit chip. (note Figures 18-20, 27 and 31)

With regard to claim 42, Murayama et al. discloses the method further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein the plurality of interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing the plurality of electronic packages from each other. (note Figures 20 and 26)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, 13-14 and 34-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (PN 6,235,552, of record) in view of Murayama et al. (PN 6,548,330). Kwon et al. discloses, as shown in Figures 19-20 and 26-27, a method of preparing a pre-formed integrated circuit chip for encapsulation in an electronic package comprising the steps of:

forming an interconnect assembly (130) separately from the pre-formed integrated circuit chip (100); (note Figures 6 and 14-15)

forming a plurality of conducive bumps (128) connected to the terminals (104) of the pre-formed integrated circuit chip,

bonding the interconnect assembly to the pre-formed integrated circuit chip; (note Figure 16)

passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into an integral structure to provide the electronic package. (note Figures 17 and 26-27)

Kwon et al. does not disclose a step of thinning the pre-formed integrated circuit chip to provide the electronic package. However, Murayama et al. discloses the methods of preparing a pre-formed integrated circuit chip comprising the step of thinning the pre-formed integrated circuit chip. Note Figures 5 and 12 of Murayama et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit chip of Kwon et al. comprising the step of thinning the pre-formed integrated circuit chip, such as taught by Murayama et al. in order to reduce the overall thickness of the electronic package.

With regard to claim 2, Kwon et al. and Murayama et al. disclose the step of forming the interconnect assembly comprises forming the interconnect assembly on a releasable substrate (110).

With regard to claim 3, Kwon et al. and Murayama et al. disclose the step of forming the interconnect assembly comprises forming at least one pad (116) in an interconnect layer, which at least one pad can be accessed and electrically connected on opposing side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 4, Kwon et al. and Murayama et al. disclose the step of forming at least one test pad forms a test pad having gold on a conductive field metal. (note Col. 3, lines 46-65 and Col. 4, lines 9-13)

With regard to claim 5, Kwon et al. and Murayama et al. disclose the step of forming the interconnect assembly comprises forming at least one pad (116) in a plurality of stacked interconnect layers, each of which at least one pad in each interconnect layer can be accessed and electrically connected on opposing side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 6, Kwon et al. and Murayama et al. disclose the step of forming at least one test pad in the plurality of stacked interconnect layers forms at least one test pad in each layer having gold on a conductive field metal.

With regard to claim 7, Kwon et al. and Murayama et al. disclose the step of forming the plurality of conductive bumps connected to the terminals of the integrated circuit chip forms a metallic bump making connecting to a terminal o the integrated circuit chip and a solder layer (108) disposed on the metallic bump.

With regard to claim 8, Kwon et al. and Murayama et al. disclose the step of forming the interconnect assembly comprises forming at least one pad (116) in an interconnect layer, which at least one pad can be accessed and electrically connected on opposing side of the pad, and wherein the step of bonding the interconnect assembly to the pre-formed integrated circuit chip flip bonds the solder layer onto one side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 9, Kwon et al. and Murayama et al. disclose the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises underfilling the pre-formed integrated circuit chip with an insulating material (134,156) to remove all voids between the pre-formed integrated circuit chip and the interconnect assembly.

With regard to claims 10 and 11, Kwon et al. and Murayama et al. disclose the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the

integral structure to provide the electronic package comprises potting (by layer 156) the interconnect assembly and the pre-formed integrated circuit chip into an integral package.

With regard to claim 13, Kwon et al. and Murayama et al. disclose the method further comprising a step of accessing the pre-formed integrated circuit chip through electrical connect to at least one pad through a surface thereof opposing the surface of the at least one pad contacting a terminal of the pre-formed integrated circuit chip. Note that the pad is capable to function as a test pad. Also, the pad is capable to use to test the pre-formed integrated circuit chip. (note Figures 18-20, 27 and 31)

With regard to claim 14, Kwon et al. and Murayama et al. disclose the method further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein the plurality of interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing the plurality of electronic packages from each other. (note Figures 20 and 26)

With regard to claim 34, Kwon et al. and Murayama et al. disclose the at least one test pad forms a test pad having gold on a conductive field metal. (note Col. 3, lines 46-65 and Col. 4, lines 9-13)

With regard to claim 35, Kwon et al. and Murayama et al. disclose the step of forming the plurality of conductive bumps connected to the terminals of the integrated circuit chip forms a

metallic bump making connecting to a terminal o the integrated circuit chip and a solder layer (108) disposed on the metallic bump.

With regard to claim 36, Kwon et al. and Murayama et al. disclose the step of forming the interconnect assembly comprises forming at least one pad (116) in an interconnect layer, which at least one pad can be accessed and electrically connected on opposing side of the pad, and wherein the step of bonding the interconnect assembly to the pre-formed integrated circuit chip flip bonds the solder layer onto one side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 37, Kwon et al. and Murayama et al. disclose the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises underfilling the pre-formed integrated circuit chip with an insulating material (134,156) to remove all voids between the pre-formed integrated circuit chip and the interconnect assembly.

With regard to claims 38 and 39, Kwon et al. and Murayama et al. disclose the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises potting (by layer 156) the interconnect assembly and the pre-formed integrated circuit chip into an integral package.

With regard to claim 40, Kwon et al. and Murayama et al. disclose the step thinning the preformed integrated circuit chip. (note Figures 5 and 12)

With regard to claim 41, Kwon et al. and Murayama et al. disclose the method further comprising a step of accessing the pre-formed integrated circuit chip through electrical connect to at least one pad through a surface thereof opposing the surface of the at least one pad contacting a terminal of the pre-formed integrated circuit chip. Note that the pad is capable to function as a test pad. Also, the pad is capable to use to test the pre-formed integrated circuit chip. (note Figures 18-20, 27 and 31)

With regard to claim 42, Kwon et al. and Murayama et al. disclose the method further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein the plurality of interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing the plurality of electronic packages from each other. (note Figures 20 and 26)

Allowable Subject Matter

5. Claims 15-16 and 43-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an examiner's statement of reasons for allowance:

Applicant's claims 15-16 and 43-44 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed method further comprising bonding the plurality of interconnect assembly and pre-formed integrated circuit chips together to form a corresponding plurality of electronic packages and further comprising the step of testing the interconnect assembly and bonding a tested interconnect assembly in the step of bonding the interconnect assembly to the pre-formed integrated circuit chip only if the interconnect assembly tested good, as recited in claims 15 and 43.

Response to Arguments

7. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Note that the newly submitted claim 1 does not include all the limitations of the base claim and any intervening claims.

Applicant's arguments filed 05/14/03 have been fully considered but they are not persuasive.

It is argued, at page 12 of the Remarks, that Kwon et al. does not disclose the step of forming at least one test pad having gold on a conductive field metal and the use of gold is for the chip pad and not the test pad of the interconnect assembly, as claimed. This argument is not convincing because Kwon et al. discloses, at Col. 3, lines 46-65 and Col. 4, lines 9-13, the pads 116 are formed on the substrate base 110 in the same way that the UBM 108 was formed. It is inherent that the pads 116 having gold on a conductive field metal. Note that the pads are capable to function as the test pads.

It is argued, at page 12 of the Remarks, that Kwon et al. does not disclose a plurality of stacked interconnect layers. This argument is not convincing because Kwon et al. discloses, at Col. 3, lines 46-65 and Col. 4, lines 9-13, the pads 116 are formed on the substrate base 110 in the same way that the UBM 108 was formed. Kwon et al. also discloses the UBM 108 is multi-layered. Therefore, Kwon et al. clearly teaches the plurality of stacked interconnect layers.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The

examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

July 30, 2003

Tom Thomas

TOM THOMAS
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